AN2524
Application note

54 W / T5 ballast driven by the L6585D

Introduction

This application note describes a demo board able to drive a 54 W linear T5 fluorescent lamp.

The ballast control is done by the L6585D that integrates PFC and half-bridge control circuits, the relevant drivers, and the circuitry able to manage all lamp operating phases (pre-heating, ignition and run mode).

Protections against main failures (lamp disconnection, anti-capacitive mode, PFC over-voltage) are guaranteed and obtained with a minimum number of external components

After the circuit description, a short overview of the ballast performances is presented.

Fluorescent lamps are driven more and more by electronic, rather than electromagnetic ballast primarily because fluorescent lamps can produce around 10% more light for the same input power when driven above 20 KHz instead of 50/60 Hz. Operation at this frequency also eliminates both light flickering (the response time of the discharge is too slow for the lamp to have a chance to extinguish during each cycle) and audible noise.

An electronic ballast consumes less power and therefore dissipates less heat than an electromagnetic ballast. The energy saved can be estimated in the range of 20-25% for a certain lamp power.

Finally the electronic solution allows better control of the filament current and lamp voltage during pre-heating with the unquestionable benefit of increasing the mean lamp life.

Among electronic solutions for ballasts, ST proposes a new IC - the L6585D - that, embedding both the PFC and half-bridge control sections, allows designing a compact and reliable ballast with a minimum number of external components.

Figure 1. Evaluation board

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1 Application specifications

This board has been designed in order to drive a T5 54W lamp with the following characteristics:

Table 1. T5 – 54 W lamp characteristics

Input voltage [V_{AC}]	Mains freq. [Hz]	Lamp power [W]	Nom. Ignition voltage [V]	Lamp current [A]	Lamp voltage [V]
188 to 264	50	54	400	0.455	120

The board performs the lamp control in all operating phases as well as a PF pre-regulator stage. It also provides the following protections:

- PFC over voltage;
- PFC feedback disconnection;
- PFC choke saturation
- Lamp disconnection;
- Half-bridge anti-capacitive mode;
- High filament detection

Table 2. Schematic and part list

Ref.	Value
BR1	DF06S
R1, R2	3.6 M
R3, R4	910 K
R6	42.2 K
R9	13.3 K
R10, R11	820 K
R12	1.2 M
R13	47
R14	47 K
R15	62 k
R16	56 k
R17, R18	47
R19	0.82, 1 W
R20	10
R22	0.82, 1/2 W
R23	330
R26, R27	680 K
R30, R33	240 K

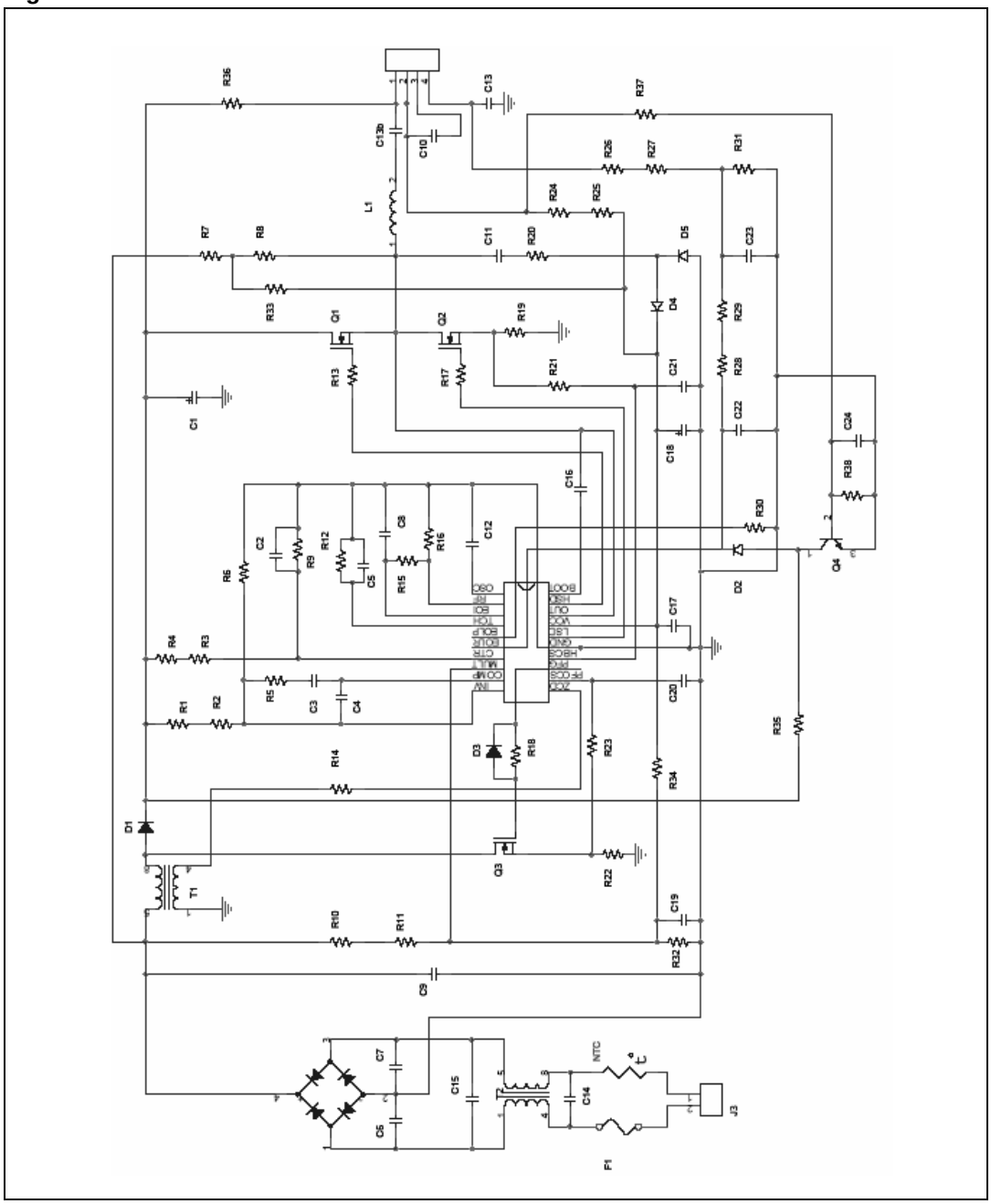
Table 2. Schematic and part list (continued)

Ref.	Value
R35	1 Mohm
R36, R37	510 K
R38	12 K
R5, R8, R24, R25, R34	n.c.
R7, R21, R28, R29	short
C1	22 µF, 450 V, EPCOS B43888A5226M9
C2, C19, C23	10 nF
C3	n.c.
C4	470 nF
C5	680 nF
C6, C7	1 nF, 1 KV
C8	330 nF
C9	470 nF, 630 V, EPCOS B32652
C10	4.7 nF, 2 kV EPCOS B32653
C11	1 nF, 630 V
C12	470 pF
C13	100 nF, 250 V
C13b	short
C14, C15	100 nF, X2, 275 Vac, EPCOS
C16, C17	100 nF
C18	10 µF, 35 V
C20	1 nF
C24	330 nF
C21, C22	n.c.
T1	E25, 2.1 mH, EPCOS B78313P7580A005 (T2363 51-03)
T2	39 mH, EPCOS B82731M2601A 30
F1	2 A fuse
RT1	NTC, 16R
D1	STTH1L06
D2	1N4148
D3	1N4148
D4	1N4148
D5	BZX84C15ZTX
L1	ITACOIL, 1.3 mH

Table 2. Schematic and part list (continued)

Ref.	Value
Q1	STP4NK50ZD
Q2	STP4NK50ZD
Q3	STD3NK50Z-1
Q4	BC817
IC1	L6585D

Figure 2. Evaluation board schematic



The PFC section provides the downstream half-bridge with a regulated output voltage of 429 V, defined by the feedback divider connected to the pin INV according to the following formula:

Equation 1

$$V_{OUT} = V_{REF} \bullet \left(1 + \frac{R1 + R2}{R6}\right) = 2.5 \bullet \left(1 + \frac{3.6M + 3.6M}{42.2K}\right) = 429V$$

where V_{REF} is the 2.5 V reference internally connected to the non inverting input of the error amplifier.

A 100 Hz ripple (twice the mains frequency) is superimposed on the regulated output voltage. The amplitude of this ripple is determined by the capacitance value of the PFC output capacitor, namely:

Equation 2

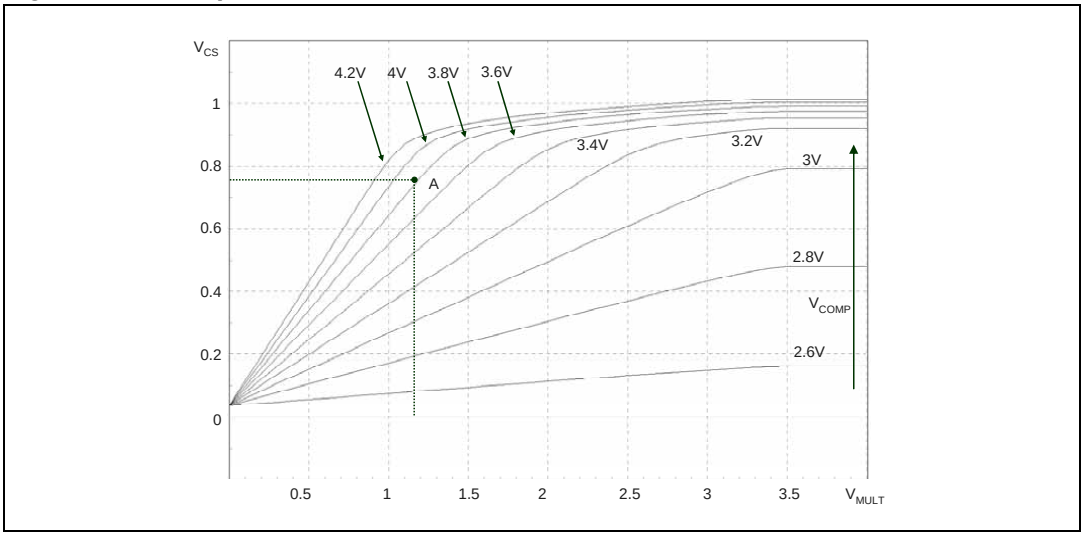
$$\Delta V_{OUT} = \frac{P_{OUT}}{4 \bullet \pi \bullet f_L \bullet V_{OUT} \bullet C_{OUT}} \approx 10V$$

where ΔV_{OUT} is one-half of the peak-to-peak ripple, P_{OUT} the estimated power at PFC output (58 W), f_L the mains frequency, V_{OUT} the PFC output DC voltage and C_{OUT} the bulk capacitor (22 µF).

To define the power that the PFC stage is able to handle, a sense resistor is connected between the Power MOSFET source and ground. Its value has been chosen supposing a global efficiency of 87%. This corresponds to an input power of 62 W leading to a choke (and Power MOSFET) peak current of 0.93 A at the minimum input voltage. The sense resistor value causes a maximum peak current of 1V/Rsns so, for a safe proper design, the saturation current of the PFC inductance must be at least equal to this value. The L6585D contains an anti-saturation circuit in order to avoid this kind of failure that could damage the PFC Power MOSFET due to high current spikes.

Using the multiplier family characteristic curves (*Figure 3*), it is possible to fix the operating point in the worst case condition, that is minimum input voltage and maximum load (point A). As a result, a resistor of 0.82Ω has been chosen.

Figure 3. Multiplier characteristics



The minimum switching frequency is set at 34 KHz. This value can be obtained by using the following formula:

Equation 3

$$F_{SW(MIN)} = \frac{V^2_{IN(RMS)} \bullet (V_{OUT} - \sqrt{2} \bullet V_{IN(RMS)})}{2 \bullet L \bullet P_{IN} \bullet V_{OUT}} = 34kHz$$

where $V_{IN(RMS)}$ is the min/max input voltage, L the inductance value and P_{IN} the input power. This value must be higher than the starter frequency whose maximum value is 15 KHz. The RMS current flowing through the Power MOSFET is equal to ~270 mA and the STP3NK50 has been chosen consequently.

- Half-bridge section

The lamp pre-heating and run frequency are set at:

Equation 4

$$F_{PRE} = \frac{k}{C_{OSC} \bullet (R_{RUN} \,||\, R_{PRE})} = \frac{1.328}{C_{12} \bullet (R_{16} \,||\, R_{15})} = 92.77kHz$$

Equation 5

$$F_{RUN} = \frac{k}{C_{OSC} \bullet R_{RUN}} = \frac{1.328}{C_{12} \bullet R_{16}} = 50.4kHz$$

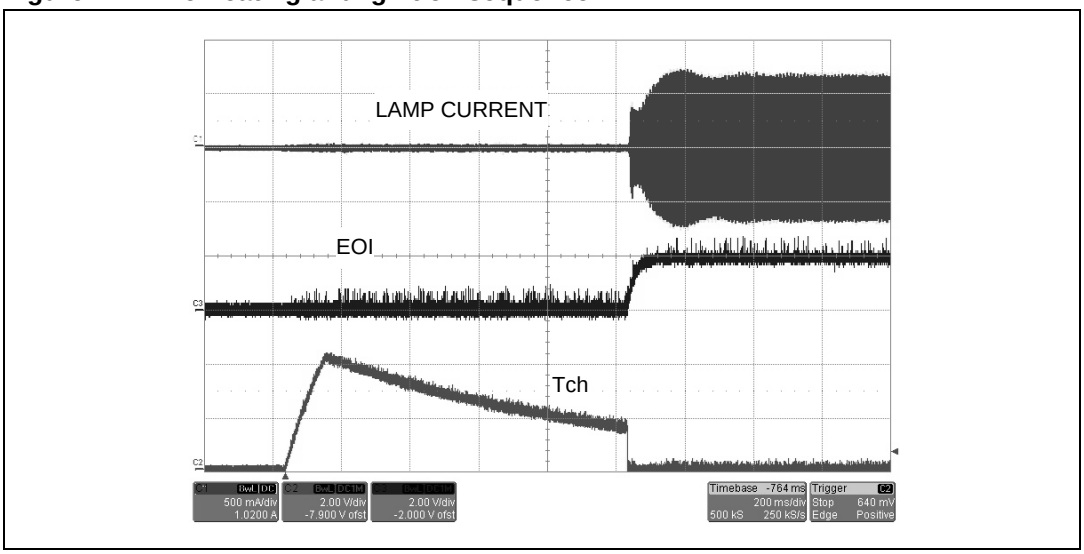
The pre-heating time duration is defined according to the following formula:

Equation 6

$$T_{PRE} = T_{CH} + T_{DISCH} = \frac{C_5}{I_{CH}} \bullet 4.63 + R_{12} \bullet C_5 \bullet \ln\left(\frac{4.63}{1.5}\right)$$

where I_{CH} is the output current on pin T_{CH} just after the start-up, 4.63 V and 1.5 V are the charge and discharge threshold respectively (see datasheet electrical characteristics). The frequency shift during ignition is steered by the time constant R_{15}-C_8. *Figure 4* shows the lamp current during the turn-on sequence (pre-heating →ignition →run mode) together with the T_{CH} and EOI signals that manage the time durations of the different phases.

Figure 4. Pre-heating and ignition sequence



A RMS current equal to ~500 mA flows through each of the half-bridge Power MOSFET and two STP4NK50Z have been chosen consequently.

2 Board performances

The PFC section operates in transition mode. The results in terms of PF and THD are shown in the following table:

Table 3. PF and THD values as a function of the input voltage

Vin [Vac]	PF	THD [%]
188	0.996	4.5
235	0.990	5.4
264	0.982	7.1

Figure 5. Input current at input voltage equal to 188 V_{AC}

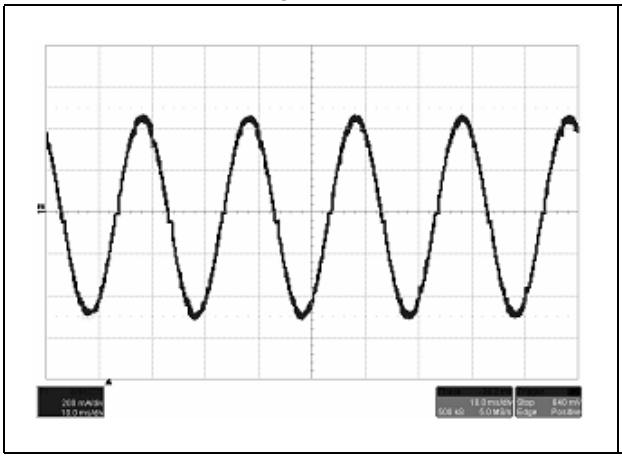
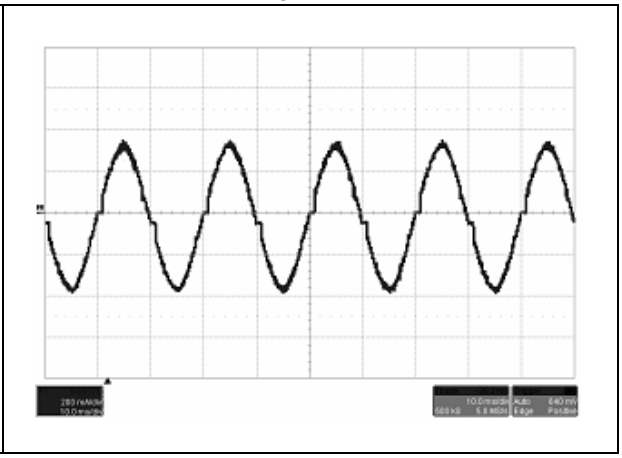


Figure 6. Input current at input voltage equal to 264 V_{AC}



3 Protections

3.1 3.1 PFC over-voltage

A resistive divider connected to the HV output bus sets the maximum allowed voltage at the PFC output at 468 V. This value can be obtained by the following formula:

Equation 7

$$V_{OV} = V_{THOV} \bullet \left(1 + \frac{R3 + R4}{R9}\right) = 468V$$

where V_{THOV} is the threshold of the comparator available at the CTR pin (3.4 V typ.). The device stops the PF gate driver until the V_{THOV} signal goes below the low threshold hysteresis (3.26 V typ.).

The above comparator is helpful in stopping the PF gate driver before the PFC output voltage reaches values that could exceed the maximum bulk capacitor voltage or the mosfets breakdown.

3.2 PFC open loop (feedback disconnection)

If instead the over-voltage is due to feedback disconnection (R1+R2 fails open), these two structures work together. In fact if the V_{OVP} threshold is crossed and simultaneously the INV voltage falls below 1.2 V, typ. (due to the fact that the E/A source capability is limited), the IC stops in a latched condition.

The CTR pin offers another comparator that is triggered when the pin voltage falls below 0.75 V (typ.). This is a not latched condition that could be used for several purposes (re-lamp, disable…). Note that this function offers complete protection against not only feedback loop failures or erroneous settings, but also against a failure of the protection itself. Either resistor of the CTR divider failing short or open or a CTR pin floating results in shutting down the IC and stopping the pre-regulator.

3.3 Choke saturation

The current sense pin voltage is not only sent to the PWM comparator (responsible for normal Power MOSFET turn-off) but also to a second comparator, whose threshold is 1.7 V (typ.), and whose function is to detect choke saturation.

The sense resistor chosen (0.82 Ω), limits the current saturation at 2.1 A (typ.)

3.4 Ignition voltage increase

By placing a resistor between the half-bridge low side and ground and sending its voltage to the pin HBCS it is possible to limit the maximum voltage that can be applied to the lamp during ignition phase (to limit component stress) as well as the minimum switching frequency (in order to avoid capacitive mode).

With the selected value for R19 (0.82), the resulting maximum voltage is around 680 V.

If the lamp fails ignition, the ballast applies to it the above voltage for a duration equal to the pre-heating time. If, after this time the lamp has not yet ignited, the IC enters low consumption mode and waits for either a re-lamp or a Mains removal before enabling a new pre-heating /ignition sequence.

3.5 Lamp power increase

If, during run mode, the current flowing through the lamp increases such that the voltage across the half-bridge sense resistor exceeds the low threshold of the HBCS pin (910 mV typ), the L6585D reacts by increasing the switching frequency. This implements a current control structure. The effect of the frequency increase is the lamp power limitation, so the structure acts like a rough closed loop with a negative feedback (power increase → current increase → switching frequency increase → power limitation). There is not a switch-off in correspondence of level crossing, but a frequency correction proportional to how much the threshold level has been crossed. This protection can face the effect appearing at lamp end-of-life known as symmetrical rectification.

3.6 Lamp disconnection

The circuit built by R35, R37, R38, C24, Q4 monitors the presence/integrity of the high filament of the lamp. In case of lamp disconnection, the base of the transistor Q4 is forced to ground so through the network R35-D2, the pin EOL-R is forced above the re-lamp comparator threshold. As the lamp is inserted, Q4 is turned-on and D is reverse-biased so the voltage at pin EOL-R is no longer affected.

- Rectifying effect (end-of-life)

By means of R30 (240 KΩ), the window comparator is set to:

- reference in tracking to CTR pin;
- window amplitude equal to 220 mV.

The resistive divider built by R3+R4 and R9 sets CTR voltage under normal condition at 2.9 V. The divider R26+R27 and R31 sets the voltage at pin EOLR at 2.9 V.

The rectifying effect causes a shift (either positive or negative) of the lamp voltage that, in turn, also shifts the DC component of the block capacitor (C13) voltage. As this value exits from the allowed window for a time longer than ~1s (equal to preheat time), the IC stops.

4 Revision history

Table 4. Revision history

Date	Revision	Changes
09-May-2007	1	First issue

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